

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A data routing unit comprising:
2 a data receiver;
3 a data transmitter; and
4 at least one set of data output lines, each of said at least
5 one set of data output lines consists of a plurality of data lines
6 and a data routing unit clock line;
7 said data transmitter generating data transmitted on said data
8 output lines synchronous with a transmitter clock signal on said
9 data routing unit clock line;
10 a bridge circuit connected to supply data to said data
11 receiver and to receive data from said data transmitter, said
12 bridge circuit connected to at least one set of data input lines
13 and to said at least one set of data output lines, said bridge
14 circuit responsive to a header of a data packet received from said
15 data transmitter or received from said at least one set of data
16 input lines to selectively route said received data packet to (1)
17 said data receiver circuit, (2) a selected set of said at least one
18 set of data output lines, or (3) both said data receiver circuit
19 and a selected set of said at least one set of data output lines
20 dependent upon said header;
21 an input/output memory connected to said data receiver for
22 storing data received by said data receiver and to said data
23 transmitter for storing data to be transmitted by said data
24 transmitter; and
25 a central processing unit connected said input/output memory
26 for storing data into said input/output memory and reading data
27 from said input/output memory, said central processing unit

28 operating in synchronism with a CPU clock which is asynchronous
29 with said transmitter clock signal.

2 and 3. (Canceled)

1 4. (Original) The data routing unit of claim 1, wherein:
2 said at least one set of data input lines consists of a right
3 set of data input lines and a left set of data input lines; and
4 said at least one set of data output lines consists of a right
5 set of data output lines and a left set of data input lines.

5 and 6. (Canceled)

1 7. (Currently Amended) ~~The A~~ data routing unit of ~~claim 1,~~
2 wherein comprising:
3 a data receiver;
4 a data transmitter;
5 at least one set of data input lines, each of said at least
6 one set of data input lines consists of a plurality of data lines
7 and a data routing unit clock line; ~~and~~
8 said data receiver sensing data received on said data lines
9 synchronous with a transmitter clock signal on said data routing
10 unit clock line;
11 a bridge circuit connected to supply data to said data
12 receiver and to receive data from said data transmitter, said
13 bridge circuit connected to said at least one set of data input
14 lines and at least one set of data output lines, said bridge
15 circuit responsive to a header of a data packet received from said
16 data transmitter or received from said at least one set of data
17 input lines to selectively route said received data packet to (1)
18 said data receiver circuit, (2) a selected set of said at least one
19 set of data output lines, or (3) both said data receiver circuit

20 and a selected set of said at least one set of data output lines
21 dependent upon said header;
22 an input/output memory connected to said data receiver for
23 storing data received by said data receiver and to said data
24 transmitter for storing data to be transmitted by said data
25 transmitter; and
26 a central processing unit connected said input/output memory
27 for storing data into said input/output memory and reading data
28 from said input/output memory, said central processing unit
29 operating in synchronism with a CPU clock which is asynchronous
30 with said transmitter clock signal.

8. (Canceled)

1 9. (Currently Amended) ~~The A data routing unit of claim 1,~~
2 wherein comprising:
3 a data receiver;
4 a data transmitter;
5 a bridge circuit connected to supply data to said data
6 receiver and to receive data from said data transmitter, said
7 bridge circuit connected to at least one set of data input lines
8 and at least one set of data output lines, said bridge circuit
9 responsive to a header of a data packet received from said data
10 transmitter or received from said at least one set of data input
11 lines to selectively route said received data packet to (1) said
12 data receiver circuit, (2) a selected set of said at least one data
13 output lines, or (3) both said data receiver circuit and a selected
14 set of said at least one set of data output lines dependent upon
15 said header;
16 said bridge circuit further includes
17 a node address register storing a uniquely assigned
18 multibit node address;

19 a node address comparator connected to said node address
20 register for comparing predetermined destination node address
21 bits of said header with said node address stored in said node
22 address register; and

23 said bridge circuit selectively routing said received
24 data packet to said data receiver when said destination node
25 address bits matches said node address;

26 a plurality of routing registers, each routing register
27 corresponding to one set of data output lines, each routing
28 register storing an indication of a set of node addresses;

29 a plurality of routing comparators, each routing
30 comparator connected to a corresponding routing register for
31 comparing predetermined destination node address bits of said
32 header with said indication of as set of node addresses stored
33 in said corresponding routing register; and

34 said bridge circuit selectively routing said received
35 data packet to a set of data output lines when said
36 destination node address bits matches a node address of said
37 set of node addresses stored in said corresponding routing
38 register.

10. (Canceled)

1 11. (Currently Amended) ~~The A data routing unit of claim 9,~~
2 wherein comprising:

3 a data receiver;

4 a data transmitter;

5 at least one set of data input lines, said at least one set of
6 data input lines consists of a right set of data input lines and a
7 left set of data input lines;

8 at least one set of data output lines, said at least one set
9 of data output lines consists of a right set of data output lines
10 and a left set of data input lines;

11 a bridge circuit connected to supply data to said data
12 receiver and to receive data from said data transmitter, said
13 bridge circuit connected to said at least one set of data input
14 lines and said at least one set of data output lines, said bridge
15 circuit responsive to a header of a data packet received from said
16 data transmitter or received from said at least one set of data
17 input lines to selectively route said received data packet to (1)
18 said data receiver circuit, (2) a selected set of said at least one
19 data output lines, or (3) both said data receiver circuit and a
20 selected set of said at least one set of data output lines
21 dependent upon said header;

22 said bridge circuit further includes

23 a right routing register storing a right routing data
24 word having a plurality of bits, each bit corresponding to a
25 unique node address and having either a first digital state
26 indicating routing via said right data output lines to reach
27 said unique node address or a second digital state indicating
28 not routing via said right data output lines to reach said
29 unique node address;

30 a left routing register storing a left routing data word
31 having a plurality of bits, each bit corresponding to a unique
32 node address and having either a first digital state
33 indicating routing via said left data output lines to reach
34 said unique node address or a second digital state indicating
35 not routing via said left data output lines to reach said
36 unique node address;

37 a decoder receiving said header for converting said
38 destination node address into a multibit destination data word
39 having a bit corresponding to said destination node address in

40 said first digital state and all other bits in said second
41 digital state;
42 a right comparator connected to said right routing
43 register and said decoder for comparing said right routing
44 data word and said destination data word; and
45 a left comparator connected to said left routing register
46 and said decoder for comparing said left routing data word and
47 said destination data word; and
48 said bridge circuit selectively routing said received
49 data packet to said right data output lines when said
50 destination data word matches said right routing data word and
51 selectively routing said received data packet to said left
52 data output lines when said destination data word matches said
53 left routing data word.

1 12. (Original) The data routing unit of claim 11, further
2 comprising:
3 an input/output memory connected to said data receiver for
4 storing data received by said data receiver and to said data
5 transmitter for storing data to be transmitted by said data
6 transmitter; and
7 a central processing unit connected said input/output memory
8 for storing data into said input/output memory and reading data
9 from said input/output memory, said central processing unit
10 operable to write data into said right routing register and into
11 said left routing register.

1 13. (Currently Amended) ~~The A~~ data routing unit ~~of claim 1,~~
2 wherein comprising:
3 a data receiver;
4 a data transmitter;

5 at least one set of data input lines, said at least one set of
6 data input lines consists of a right set of data input lines and a
7 left set of data input lines;

8 at least one set of data output lines, said at least one set
9 of data output lines consists of a right set of data output lines
10 and a left set of data input lines;

11 a bridge circuit connected to supply data to said data
12 receiver and to receive data from said data transmitter, said
13 bridge circuit connected to said at least one set of data input
14 lines and said at least one set of data output lines, said bridge
15 circuit responsive to a header of a data packet received from said
16 data transmitter or received from said at least one set of data
17 input lines to selectively route said received data packet to (1)
18 said data receiver circuit, (2) a selected set of said at least one
19 data output lines, or (3) both said data receiver circuit and a
20 selected set of said at least one set of data output lines
21 dependent upon said header; and

22 said bridge circuit selectively routing said received data
23 packet to said data receiver when a predetermined central
24 navigation bit of said header has a first digital state, routing
25 said received data packet with said header deleted to said right
26 set of data output line when a predetermined right navigation bit
27 of said header has said first digital state and routing said
28 received data packet with said header deleted to said left set of
29 data output line when a predetermined left navigation bit of said
30 header has said first digital state.

1 14. (New) The data routing unit of claim 7, wherein:

2 said at least one set of data input lines consists of a right
3 set of data input lines and a left set of data input lines; and

4 said at least one set of data output lines consists of a right
5 set of data output lines and a left set of data input lines.

1 15. (New) The data routing unit of claim 9, further
2 comprising:

3 an input/output memory connected to said data receiver for
4 storing data received by said data receiver and to said data
5 transmitter for storing data to be transmitted by said data
6 transmitter.

1 16. (New) The data routing unit of claim 15, further
2 comprising:

3 a central processing unit connected said input/output memory
4 for storing data into said input/output memory and reading data
5 from said input/output memory.

1 17. (New) The data routing unit of claim 9, wherein:
2 said at least one set of data input lines consists of a right
3 set of data input lines and a left set of data input lines; and
4 said at least one set of data output lines consists of a right
5 set of data output lines and a left set of data input lines.

1 18. (New) The data routing unit of claim 11, further
2 comprising:
3 an input/output memory connected to said data receiver for
4 storing data received by said data receiver and to said data
5 transmitter for storing data to be transmitted by said data
6 transmitter.

1 19. (New) The data routing unit of claim 18, further
2 comprising:
3 a central processing unit connected said input/output memory
4 for storing data into said input/output memory and reading data
5 from said input/output memory.

1 20. (New) The data routing unit of claim 11, wherein:
2 said at least one set of data input lines consists of a right
3 set of data input lines and a left set of data input lines; and
4 said at least one set of data output lines consists of a right
5 set of data output lines and a left set of data input lines.

1 21. (New) The data routing unit of claim 13, further
2 comprising:
3 an input/output memory connected to said data receiver for
4 storing data received by said data receiver and to said data
5 transmitter for storing data to be transmitted by said data
6 transmitter.

1 22. (New) The data routing unit of claim 21, further
2 comprising:
3 a central processing unit connected said input/output memory
4 for storing data into said input/output memory and reading data
5 from said input/output memory.

1 23. (New) The data routing unit of claim 13, wherein:
2 said at least one set of data input lines consists of a right
3 set of data input lines and a left set of data input lines; and
4 said at least one set of data output lines consists of a right
5 set of data output lines and a left set of data input lines.